ABSTRACT OF THE DISCLOSURE

The present application relates to a method of fabricating planar circuits using a photolithographic mask set, to the photolithographic mask set, and to a planar circuit fabricated with the photolithographic mask set. The instant invention involves separating a photolithographic mask into two parts, namely, a master mask and one or more slave masks. The master mask and the one or more slave masks form a photolithographic mask set that is used iteratively to fabricate the planar circuits. In particular, the master mask is used as a template to provide the general layout for the planar circuit, while each slave mask is varied to tune and/or tailor the planar circuit. Since only a small portion of the planar circuit is redesigned and/or rewritten as a new mask (i.e., the slave mask), the instant invention provides a simple and cost effective method for optimizing planar circuits. Furthermore, since most mask errors will originate from the master mask, the instant invention provides an efficient method of correcting errors on planar circuits using the one or more slave masks.